THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 22

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte NORIYUKI TANINO and
YOSHINOBU SASAKI

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Appeal No. 96-1413
Application 08/134,798[1]

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ON BRIEF

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Before THOMAS, JERRY SMITH and CARMICHAEL, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

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[1] Application for patent filed October 12, 1993.

Appellants have appealed to the Board from the examiner's final rejection of claims 1 to 10, which constitute all the claims in the application.

Representative claim 1 is reproduced below:

1. A method of designing the layout of milliwave and microwave integrated circuits using a computer aided design system comprising:

displaying each a plurality of kinds of lumped circuit elements and distributed constant transmission lines for an integrated circuit on a cathode ray tube display as respective closed drawing objects, each closed drawing object having an area and dimension representing electrical data and edges for overlapping respective edges of other drawing objects to establish electrical connections between respective lumped circuit elements and transmission lines represented by corresponding drawing objects;

connecting the closed drawing objects displayed on the cathode ray tube display by overlapping the edges but not the areas of respective pairs of a plurality of the closed drawing objects to produce a virtual integrated circuit having the circuit construction of the integrated circuit; and

performing logical operations on the drawing objects of the virtual integrated circuit according to a design rule defined in accordance with a production process for producing the integrated circuit to produce at least one mask pattern for manufacturing the integrated circuit.

The following references are relied on by the examiner:

Chao et al. (Chao)	5,031,111	Jul. 09, 1991

Shikata et al. (Shikata) 5,309,371 May 03, 1994

Claims 1 to 10 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner relies upon Chao in view of Shikata.

Rather than repeat the positions of the appellants and the examiner, reference is made to the briefs and the answer for the respective details thereof.

OPINION

Generally for the reasons expressed by the examiner in the answer, and for the additional reasons presented here, we will sustain the prior art rejection of claims 1 to 10 under 35 U.S.C. § 103. Inasmuch as no arguments are presented as to any claim on appeal, and page 7 of the principal Brief on appeal indicates that all claims stand or fall together, we will consider only the features recited in representative independent claim 1 on appeal.

We agree with the appellants' and the examiner's assessment of Chao that this reference does not teach the display and overlapping of the closed circuit object edges.

On the other hand, we agree with the examiner's assessment of Shikata and the reasoning advanced at pages 4, 6 and 7 of the answer as to why it would have been obvious for the artisan to have utilized the teachings of Shikata in a combined structure to arrive at the subject matter of representative claim 1 on appeal.

Representative claim 1 recites in part that each closed drawing object has two parts, an area representing the electrical data and edges for overlapping respective edges of other drawing objects. The language of representative claim 1 in dispute between the examiner and appellants is that respective pairs of a plurality of the closed drawing objects are connected "by overlapping the edges but not the areas of the respective pairs." For the most part appellants' disclosure indicates that the overlapping of edges but not the areas of respective pairs of closed drawing objects means plainly what these words state. The disclosure also means and appellants' arguments in the brief and reply brief also indicate that the overlapping of edges means no overlapping at all, that is, that edges of pairs of closed drawing objects abut each other, are contiguous or are tangential such that

edges of adjacent pairs of closed drawing objects would touch each other. The bottom of page 1 of the reply brief states that the "entire thrust of the invention is the connection of the closed drawing objects along edges, i.e., lines."

Following this line of argument of appellants, it appears that in appellants' prior art Fig. 19(b) "the areas" of the drawing objects do in fact overlap each other but only the edges abut each other in prior art Fig. 19(a). Therefore, to the extent argued, appellants' claims would appear to read upon their own prior art Fig. 19(a). In the same sense, Fig. 19(a) appears to be consistent with the bulk of appellants' characterizations of the manner in which the connectivity is achieved in Fig. 4. In each of the graphical depictions there in the example of the connection portion of Fig. 4 for each of the active circuit elements or closed drawing objects depicted, other than the one for the resistor, the connection is achieved by abutting, or contiguous or tangential edges touching each other. Only in the resistor depiction at the top of Fig. 4 is the characterization shown for both an abutment of the resistor portion with the micro strip line on the left with an apparent overlapping of the "area" portion of

the micro strip line on the right. In this sense then, appellants' own disclosed invention appears to read upon and be consistent with the disadvantages asserted to exist with the area overlap of Fig. 19(b). In the same sense, the bulk of appellants' Fig. 4 other than the depiction for the resistors appears to be consistent with appellants' characterization of the prior art in Fig. 19(a).

With this understanding in mind, appellants' characterization that Shikata overlaps the "area" of drawing objects is misplaced. At the top of page 9 of the principal Brief on appeal appellants characterize the figures 8 to 13 of Shikata as including showings that some intersections of areas of closed drawing objects representing circuit elements are shown. By the use of the word "some" appellants impliedly admit there is some showing of a tangential or edge only connection in these figures, which is consistent with our view of the same figures.

From our study of this reference, it appears to us that the Fig. 7 showing in Shikata shows the overlapping of areas in some cases as well as the tangential connectivity of certain ones of the elements at the edges only. After the

compaction procedures as taught in this reference the Fig. 8 showing would appear to indicate that there is an overlapping of some edges only, no overlapping of areas, the absence of any overlap at all and in some cases a tangential or edge abutment connection. The shape altered version of Fig. 8 in Fig. 9 does not show any overlapping areas, shows tangential or abutting connected areas as well as some areas that are not connected at all. The final aspect ratio adjusted depiction for this first embodiment in Shikata's Fig. 11 appears to us to show the contiguity or abutment between the edges of closed drawing figures, the absence of some of them touching at all and a possible overlapping of edges between items 2 and 4, for example. Similar assessments can be made with respect to Figs. 19, 20, 24 and even Shikata's assessment of the prior art at Fig. 41.

With respect to the Fig. 15B flowchart, the determination of whether any overlap exists at block 2140 is explained at col. 13, lines 40 through 59 such that a predetermined value of the overlap may equal zero. In this case, all of the respective closed drawing objects would have no overlap at all in their final version and would therefore abut or be

tangentially connected with respect to objects adjacent other drawing objects. There are compelling repetitive teachings in Shikata's specification against any overlap among the area portion of the respective drawing objects, but according to this formula at Fig. 15B some minor overlap may exist according to the actual value the artisan would choose to prescribe for the value of H_1. In this case, should it exist, there would be no overlapping of "areas" as we understand it is intended in claim 1 and from appellants' disclosure, but only an overlap of edge portions or edge regions.

In view of the foregoing, the decision of the examiner rejecting claims 1 to 10 under 35 U.S.C. § 103 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

JAMES D. THOMAS Administrative Patent Judge	)
JERRY SMITH Administrative Patent Judge	) BOARD OF PATENT) APPEALS AND) INTERFERENCES
JAMES T. CARMICHAEL Administrative Patent Judge	)

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